A High Voltage Pulse Generator Based on Sequentially Charged Modular Multilevel Converter Sub-modules Operating in a Voltage Boost Mode

Mohamed A. Elgenedy [1,2*], A. Darwish [3*], Shehab Ahmed[4] , Barry W. Williams[5], J. R. McDonald[5]

[1] Current affiliation: Electronic and Electrical Engineering, Strathclyde University, Glasgow G1 1RD, UK
[2] Electrical Power Engineering, Alexandria University, Alexandria, Egypt
[3] Electrical Engineering, Lancaster University, LancasterLA1 4YR, UK
[4] Electrical and Computer Engineering, Texas A&M University at Qatar, Doha, Qatar
[5] Electronic and Electrical Engineering, Strathclyde University, Glasgow G1 1XW, UK
[*] mohamed.elgenedy@strath.ac.uk

Abstract: Pulse forming networks and Marx generators are the classical rectangular waveform pulse generators (PGs). They are inflexible and their capacitors must be fully charged to the required voltage from 0V before delivering each high-voltage (HV) pulse. They are only able to generate unipolar pulses; if bipolar pulses are sought another generator fed from a negative supply voltage is added. Recently, several power electronics based PGs have been proposed. This paper presents an HV power electronics based PG, which is based on Half-Bridge Modular Multilevel Converter (HB-MMC) sub-modules (SMs) charged sequentially in a voltage boost mode. Each SM capacitor and main switch form a boost converter with the charging input supply and inductor. As a result, all SM capacitors are charged to a voltage greater than the input. During the discharging process the SM capacitors are connected in series, producing a rectangular HV pulse across the load. The proposed charging method allows a reduction in the converter footprint in comparison with recently proposed MMC sequentially charged PG topologies. Although only rectangular pulse waveforms are sought in this paper, a SM capacitor voltage balance method allows multilevel pulse generation. The viability of the proposed converter is confirmed by MATLAB/Simulink simulation and scaled-down experimentation.

Nomenclature

C_{SM}	MMC-SM capacitance (F)
E_s	pulse energy (J)
E_L	energy delivered to the load (J)
I_L	input inductor current (A)
L_i	input inductance (H)
N	number of MMC SMs
r_c	charging resistance (Ω)
R	load resistance (Ω)
T_s	pulse repetition time
T_m	MMC-SM main IGBT switch
T_x	MMC-SM auxiliary IGBT switch
t_L	input inductor energising time (s)
t_C	MMC-SM capacitor charging time (s)
t_p	positive pulse polarity duration (s)
t_n	negative pulse polarity duration (s)
t_{pz}	zero load voltage duration after +ve pulse (s)
t_{nz}	zero load voltage duration after -ve pulse (s)
t_{pl}	widest pulse polarity duration (s)
V_s	DC input voltage (V)
V_P	pulse peak voltage (V)
β	per unit capacitor remaining voltage after pulse
λ	voltage boosting factor

1. Introduction

In most electroporation applications a rectangular High Voltage (HV) Pulse Generator (PG) is essential. The attractive features of rectangular pulse waveforms are their generation simplicity and effective pulse area [1]-[2]. Usually, charging a group of capacitors in parallel then discharging them in series provides HV pulses between the connecting load terminals. This concept is used in classical HV PGs such as the Marx generator (MPG), shown in Fig. 1a, and Pulse Forming Networks (PFNs) shown in Fig. 1b. In the MPG the HV pulse is formed when cascaded voltage break down of the spark gaps results in connecting (and discharging) the charged capacitors in series [3].

If faster and shorter pulses are required, the charging resistances are reduced. The trailing edge nature of the generated HV pulse in the MPG is exponential. If near rectangular pulses are required, PFNs can be used. The PFN is formed of N cascaded LC sections, as illustrated in Fig. 1b, connected to an input voltage source V_s. After storing the energy in the LC branches, an HV switch is closed across the load (after disconnecting the input supply), such that the required pulse voltage is delivered [3]-[7].

The spark gaps can be replaced by semi-conductor switches, forming the so-called solid-state MPG (SMPG). Thus, a controllable capacitor charging/discharging mechanism is possible. There are several SMPG variations, all sharing the original MPG concept of charging (in parallel) and discharging (in series) the capacitors [8]-[14]. SMPGs alleviate the need to fully discharging the capacitors before re-charging them. However, SMPG topologies suffer from significant capacitor voltage droop after pulse generation, hence droop control mitigation is inevitable [15]. An example of an SMPG topology is given in Fig. 1c where switches S allow parallel charging of the capacitors while switches T allow pulse generation across the load [14].

The Marx generator structure is inflexible, while the solid state based version lacks modularity as different solid state switch ratings are mandatory. The PFN has a fixed HV pulse width based on the selected LC values.

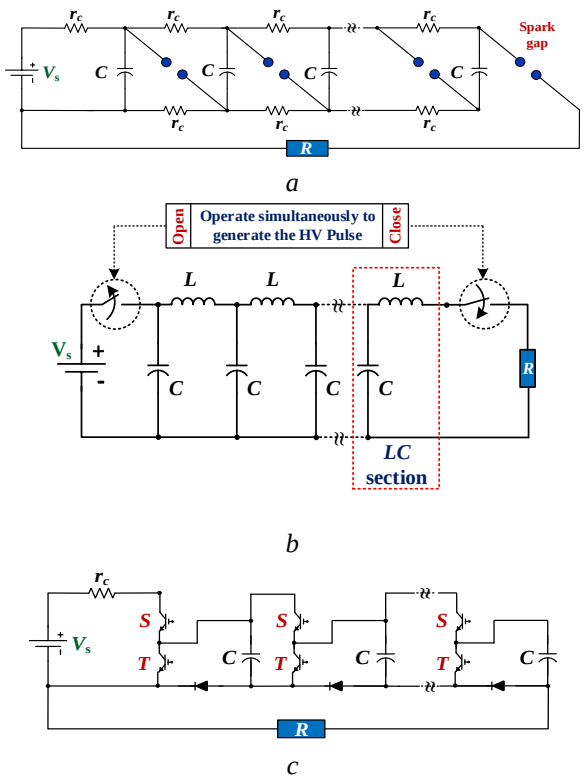


Fig. 1. *Traditional PG topologies*
(a) Classical Marx generator, **(b)** Pulse Forming Network, and **(c)** Solid-state Marx generator.

With the advantage of generating HV pulses from a relatively low voltage DC (LV DC) input, several power electronics based topologies appear in the literature. In [16], a flyback converter is modified by removing the output filter capacitor and adding an RCD circuit across the transformer primary side. A negative unipolar HV pulse is generated across load, with further voltage step up due to the transformer turns ratio. In [17] a parallel and series combination of flyback converters is utilized for HV pulse generation. In [18], an input buck-boost converter feeds a stack of LV switch–capacitor units at the output stage. With control of the series switches, an HV pulse is impressed across the load with controllable dv/dt. An LV DC source followed by a Capacitor-Diode-Voltage Multiplier (CDVM) stage is used for HV pulse generation in [19]-[20].

Recent topologies exploit the inherited capacitance in modular multilevel converter (MMC) sub-modules (SMs), in both half and full bridge versions, to generate HV pulses [21]-[30]. Such PGs, can generally be divided in two input source groups, regardless their structure, namely: HV DC fed PGs and LVDC fed PGs. Each offers merits and demerits in terms of controllability, voltage stresses across the semi-conductor switches, and flexibility of the generated pulse waveform shape and polarity, as detailed in [30].

The MMC phase-leg, Fig. 2a, fed from HV DC supply has been researched [21]-[25]. However, phase-leg MMC PGs fed from an HV DC input, V_s , generally suffer from the following limitations:

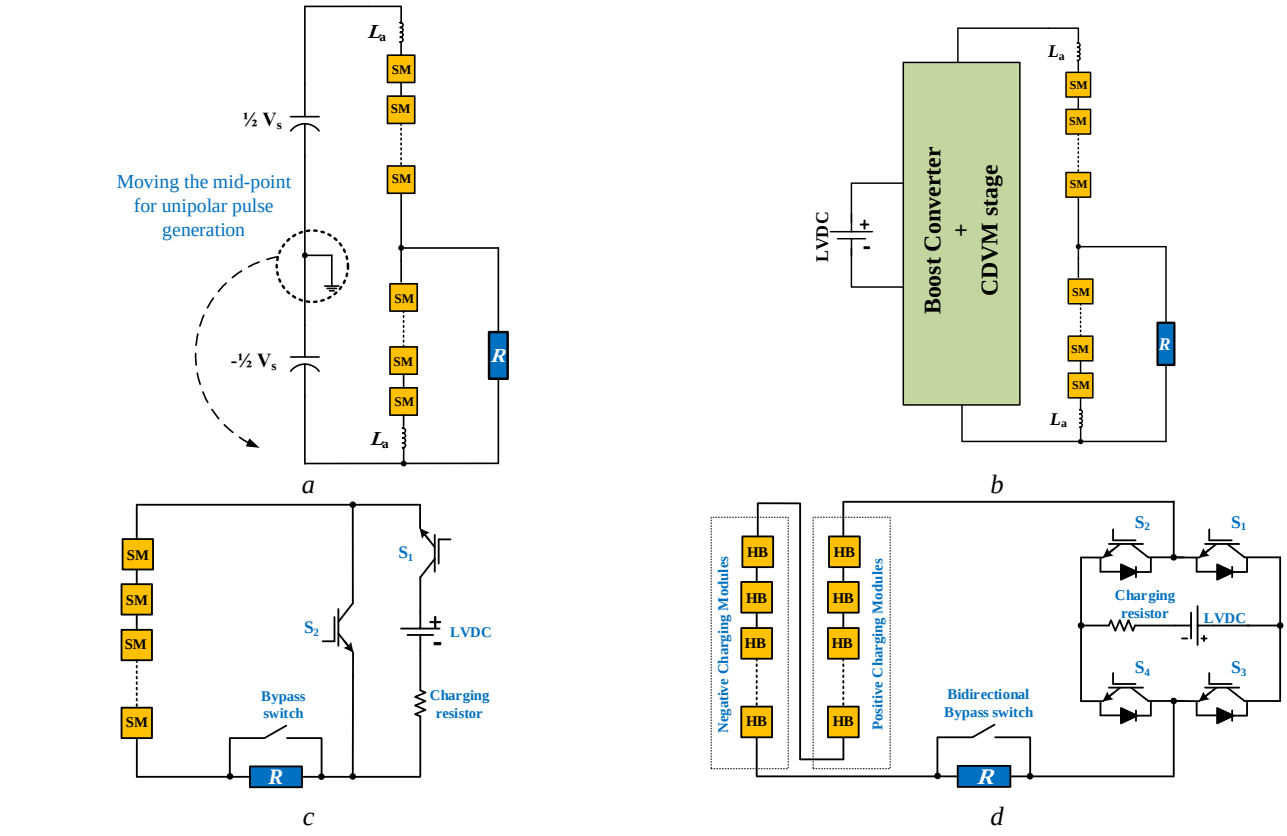


Fig. 2. *MMC PG topologies*
(**a)** MMC Phase-leg PGfed from HV DC supply, **(b)**LV DCsupply MMC fed phase-leg PG, **(c)** and **(d)**Sequential charging MMC SMs fed from LV DC supply.

- Need for an HV DC input, as the MMC cannot boost the input voltage.
- SM capacitor voltage balancing is essential.
- Large footprint.
- Generated pulses are bipolar with the default connection, however, for unipolar pulses the reference point is moved to ground. Thus the converter cannot generate both bipolar and bipolar pulses without physical power hardware changes.

Several approaches have been introduced to alleviate the need of the HV DC input while benefiting from the use of MMC SMs. A boost converter fed from an LV DC source followed by a CDVM stage is proposed in [26] such that HV DC is obtained, as shown in Fig. 2b. The generated HV DC is then applied at the terminals of a phase-leg MMC. In [27], a specific number of HB-SMs (according to the required pulse peak voltage) are charged sequentially from an LV DC input then discharged in series across the load, forming unipolar HV pulses, as shown in Fig. 2c. During progressive sequential SM charging, the charging SM is inserted while the other series SMs are bypassed, whereas, the load is bypassed and switches S_1 and S_2 are turned ON and OFF, respectively. During HV pulse generation, all the charged SMs are inserted simultaneously and switches S_1 and S_2 are turned OFF and ON, respectively, thus, a unipolar rectangular HV pulse appears across the load. But the charging mechanism is achieved via a relatively high charging resistance to limit the charging current. Consequently, capacitor charging time is elongated, which limits the pulse generation repetition rate and/or the number of utilized SMs. In [28], the HB-SMs are replaced with FB-SMs to allow bipolar HV pulses generation across the load. Alternatively, two groups of series connected HB-SMs are employed in [29], such that one group is responsible for generating the positive pulse polarity and the other generates the negative pulse polarity. Charging the HB-SMs in each group is possible by using an H-bridge across the LV DC supply and the charging resistor as shown in Fig. 2d. In [30], the sequential charging is achieved by a series rL branch which increase the control degree of freedom and allows flexible pulse generation.

The maximum obtained pulse peak-voltage from the mentioned sequential charging topologies [27]-[30] is limited by the number of SMs, N. If each SM-capacitor is charged to V_s, the pulse peak voltage is NV_s. As a result, for a fixed LV DC input, the only available option to increase the pulse voltage is to increase the number of SMs. This adversely affects pulse repetition time, as the individual SMs are charged sequentially, which increases converter footprint. In order to achieve both high voltage gain and high repetition rate, with the same or even reduced footprint, in comparison with conventional sequential charging PGs, this paper introduces a control variable to allow variable HV generation. The introduced control variable is gained by allowing the individual SMs to operate in a voltage boost mode, that is, each SM acts as a boost converter when inserted sequentially in series with input dc supply V_s and the energizing inductor L_i in Fig. 3a.

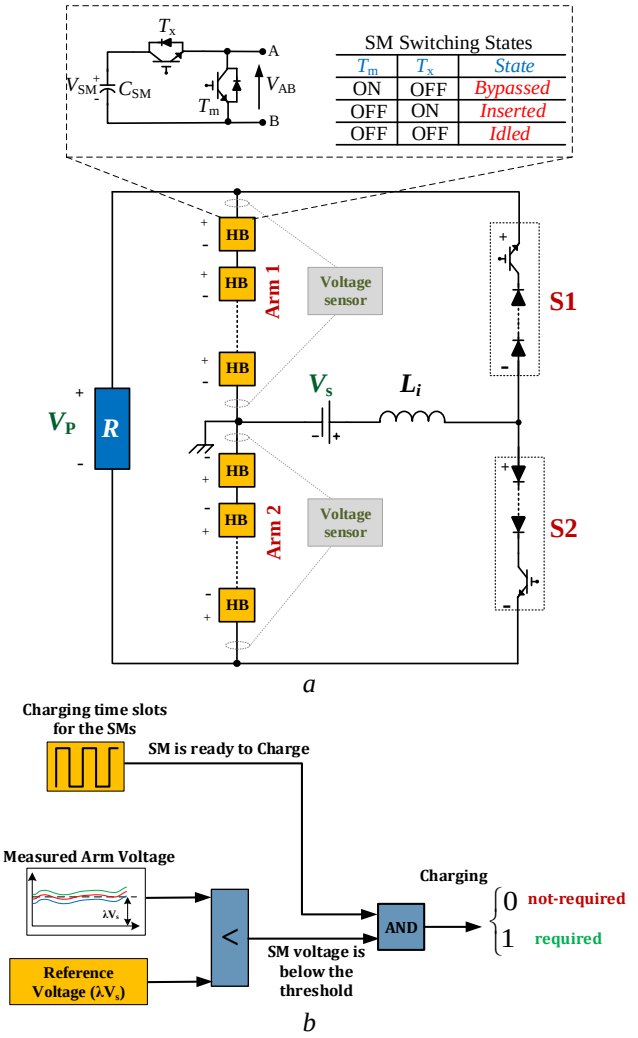


Fig. 3. *Proposed BMPG*
(a) Converter topology and **(b)** Modified SM-capacitors charging mechanism to avoid capacitor voltage drift in generic pulse wave form mode.

Although the targeted pulse waveform in this paper is rectangular, the proposed PG can operate in a generic pulse waveform mode. A new voltage balancing technique is introduced to overcome capacitor voltage drift in the generic pulse waveform mode, using only one voltage sensor per MMC arm.

Since rectangular pulse waveforms dominate pulse power applications, this paper introduces a new compact rectangular waveform PG. The proposed PG is able to generate the required rectangular pulses with reduced footprint in comparison with similar MMC based PGs. The main contributions of the proposed voltage boost mode pulse generator (BMPG) can be summarized as:

- HV pulse generation from an LV DC input supply.
- No capacitor voltage droop mitigation is required.
- Flexible and controllable rectangular pulse-waveform generation.
- Bipolar/unipolar pulse generation.
- No individual SM voltage sensors.
- No capacitor voltage drift, with only one voltage sensor per arm.

- Extendable to operate in a generic pulse wave generation mode by utilizing one voltage sensor per arm.
- Scalability by increasing the number of SMs and/or increasing the boost factor.

However, the proposed BMPG has the following operation limitation:

- Increasing the number of SMs adversely affects the pulse repetition rate.
- Since the pulse generation is software controlled, a fast controller is required.
- The two required voltage sensors for extending operation to generic pulse waveform need HV isolation and high band width.

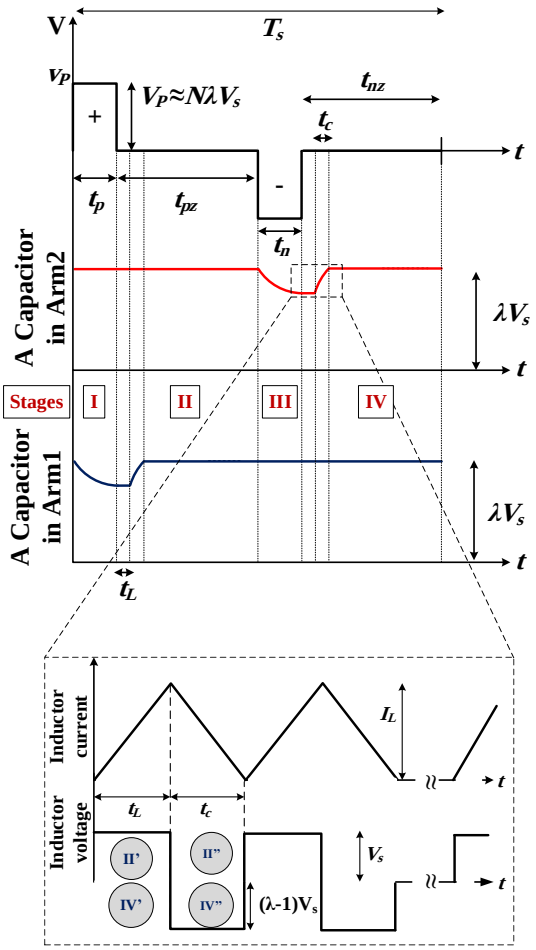
2. BMPG Topology Operation Principle

The proposed BMPG topology, shown in Fig. 3a, is comprised of two series-connected HB-SM arms (Arm1 and Arm2) and two series-connected IGBT-diode switches (S1 and S2). The arrangement of SMs and series IGBT-diode switches (S1 and S2) is such that the individual capacitors of the upper *N* series-connected SMs, Arm1, are charged to $+\lambda V_s$ through S1 from the LV input supply V_s. The individual capacitors of the lower *N* series-connected SMs, Arm2, are charged through S2 from the same LV input supply V_s but are charge to a reverse polarity. The reverse blocking switches S1 and S2 allow individual SM capacitor sequential charging as well as providing a closed loop path to energize the input inductor, L_i, creating a voltage-boost mode for SM-capacitor charging. These two switches are exposed to a reverse high voltage during pulse generation, hence reverse blocking switches (series connected diodes) are required [17]. The proposed topology requires no voltage sensors for generating HV bipolar rectangular pulses. Generation of multilevel pulse waveforms is possible assuming identical SM-capacitors. Practically, capacitances differ, which will eventually lead to capacitor voltage drift. A remedy is to use a voltage sensor across each arm as illustrated in Fig. 3a. The measured voltage is compared with a reference voltage; a SM capacitor is only re-charged if its voltage is below the reference during its allocated charging slot, as illustrated in Fig. 3b.

2.1. SM Capacitors Charging and Discharging Sequence

In order to generate the required HV pulses across the load *R*, in Fig. 4, the following operational sequence assumes the SM-capacitors are initially pre-charged:

- *Positive pulse generation*: An HV pulse of positive polarity is generated across the load *R* for the required time t_p by simultaneously inserting the SM capacitors of Arm1 (T_x ON, T_mOFF). During t_p, denoted stage I in Fig 4, Arm2 SMs are bypassed (T_x OFF, T_m ON) while switches S1 and S2 are both OFF, as shown in Fig. 5a.
- *Negative pulse generation:* For a negative pulse period t_n, denoted stage III, Fig. 4a, negative pulse of peak $-N\lambda V_s$ is formed across the load by inserting Arm2 capacitors, bypassing Arm1with switches S1 and S2 OFF, as shown in Fig. 5b.
- *Arm1 capacitors voltage re-charge*: Individual SM capacitors of Arm1 are re-charged, for the next positive pulse generation, during t_{pz}, denoted stage II in Fig 4. In order to produce the voltage boost feature, this stage is divided into two sub-stages (II' and II'').
  i. *Sub-stage II'*, Fig. 5c, S1 is turned ON and the main switch of a SM in Arm1, T_m, is turned ON (as are other T_m in other SMs). Accordingly, a current I_L energizes the input inductor L_i for a pre-specified time t_L.
  ii. *Sub-stage II''*, shown in Fig. 5d, is when a switch T_m is turned OFF and inductor energy diverts current into that SM capacitor via the the SM's diode in antiparallel with T_x. This boost converter action charges the SM capacitor for a pre-designed charging time t_C.



Input inductor voltage and current during the SM capacitor charging

Fig. 4. Bipolar HVpulse generation sequence along with the SM capacitor voltage profile and the current through, and the voltage across, the energizing input inductor.

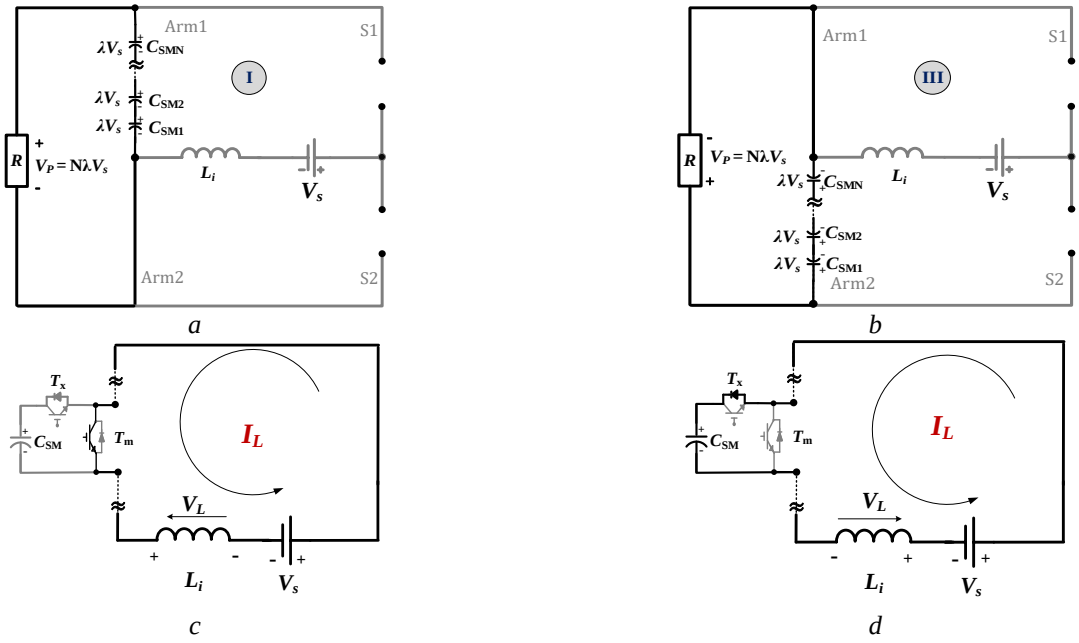


Fig. 5.*BMPGequivalent circuit*
(a) During positive pulse generation,**(b)** During negative pulse generation, **(c)** During energising L_i in sub-stages II' and IV', and **(d)** During chargingC_{SM} in sub-stages II" and IV".

The two sub-stages are repeated on each arm SM and Stage II is completed when each SM capacitor in Arm1 is charged to a dc voltage λV_s, such that λ is the voltage boost factor. The voltage across the load is zero during this SM capacitor charging process.

- *Arm2 capacitors voltage re-charge*: similar to stage II, stage IV is divided into sub-stages IV' and IV". Thus, each SM in Arm2 is used to re-energize the inductor in sub-stage IV' then a SM capacitor is re-charged in IV". Zero voltage is across the load for t_{nz}.

2.2. Adjusting the Boost factor, λ

The inductor voltage, illustrated in Fig. 4, must obey the voltage-second balance rule:

$$V_s t_L = V_s(\lambda - 1)t_c \tag{1}$$

Re-arranging yields:

$$\frac{t_c}{t_L} = \frac{1}{\lambda - 1} \tag{2}$$

The software controller determines and assigns the ratio between the time of energizing the input inductor, t_L, and the SM capacitor charging time, t_c. For example, if the SM capacitors are to be charged to twice the input LVDC voltage, then $\lambda = 2$ whence $t_L = t_c$ according to (2). As in boost converters, λ theoretically can vary between $1 < \lambda < \infty$. But the limiting factors for the available wide range of λ are dependent on the available supply voltage level, switches ratings, and circuit losses. Practically, circuit losses tend to limit the maximum boost factor to 5 to 6.

2.3. Input Inductor and SM-Capacitance Sizing

The minimum inductance is selected to control the current ripple of the charging current of the SM capacitors. Thus the inductance can be estimated from

$$L_i \geq \frac{V_s t_L}{\Delta I_L} \tag{3}$$

The SM footprint/volume of the BMPG topology is dominated by SM capacitor size. The main task of the capacitors is to provide an energy pool for pulse generation operation. After each pulse generation the energy delivered to the load must be replenished from the input supply for continuous PG operation. The pulse energy E_s for N SMs is

$$\begin{aligned} E_S &= N[½C_{SM}(\lambda V_s)^2 - ½C_{SM}(\beta\lambda V_s)^2] \\ &= ½NC_{SM}(\lambda V_s)^2(1-\beta^2) \end{aligned} \tag{4}$$

where β is the per-unit remaining voltage on each SM after pulse delivery. The variable β is a design variable to control the SM capacitance, hence physical size. The resistive load pulse energy is

$$E_L = \frac{(N\lambda V_s)^2}{R} t_{pl} \tag{5}$$

where E_L is the energy delivered by the SM capacitors into load R during pulse polarity generation and t_{pl} is the widest pulse polarity duration. Thence, the SM capacitance is

$$C_{SM} = \frac{2Nt_{pl}}{(1-\beta^2)R} \tag{6}$$

The resultant repetition rate of the generated pulses can be calculated as

$$T_s = t_p + t_n + 2N(t_L + t_c) \tag{7}$$

Table 1 BMPG simulation and experiment Specification

Parameter		Simulation	Experimental
LV DC input voltage	V_s	1 kV	50 V
Number of SMs/ Arm	N	3	3
Load resistance	R	1 kΩ	500 Ω
Input inductance	L_i	600 µH	650 µH
SM capacitance	C_{SM}	1 µF	10 µF
SM charging time	t_c	5 µs	20 µs
Pulse duration	t_{pl}	5 µs	20 µs
pu remaining voltage	β	0.99	

3. BMPG Simulation Results

MATLAB/Simulink simulations are used to assess the viability of the proposed BMPG topology, with the specifications in Table 1. With three SMs per arm and an input voltage of 1 kV, the BMPG is simulated when charging each SM capacitor to double the input voltage, that is $\lambda = 2$. Fig. 6a shows the generated bipolar pulses across the load while Fig. 6b shows the SM capacitor voltages for Arm1. Since the boost factor is 2, each SM-capacitor is charged to 2 kV, and the peak of the generated pulse is 6 kV with $T_s = 70$µs, as shown in Fig. 6a. Fig. 6c shows the input inductor current with equal charging and discharging times, $t_L = t_c$.

For $\lambda = 3$, the energizing time of the inductor is increased such that $t_L/t_c = 2$ according to (2). Fig. 7a shows the output voltage pulse which has a 9kV peak and $T_s = 100$µs repetition time. The SM capacitor charging voltage is three times the input supply, 3 kV, as shown in Fig. 7b. The input inductor current is shown in Fig. 7c.

The proposed charging mechanism, illustrated in Fig. 3b, to avoid capacitor voltage drift is simulated when the SM capacitances are mismatched. With $\lambda = 2$ and $V_s = 1$kV, the positive arm is programmed to generate multilevel pulse whereas the negative arm is programmed to generate rectangular pulse. The capacitances of the three SMs either in the upper or the lower arm are mismatched as follows 8µF, 10µF and 12µF (viz. ±20% deviation from the nominal 10µF). Each SM capacitor is expected to fluctuate around 2kV and the pulse peak-voltage is expected to be 6kV. Fig. 8a shows the train of the generated pulses before and after applying the proposed controlled charging mechanism, which uses one voltage measurement transducer per arm. The corresponding SM capacitor voltages of the positive and negative arms are shown in Fig. 8b and Fig. 8c, respectively.

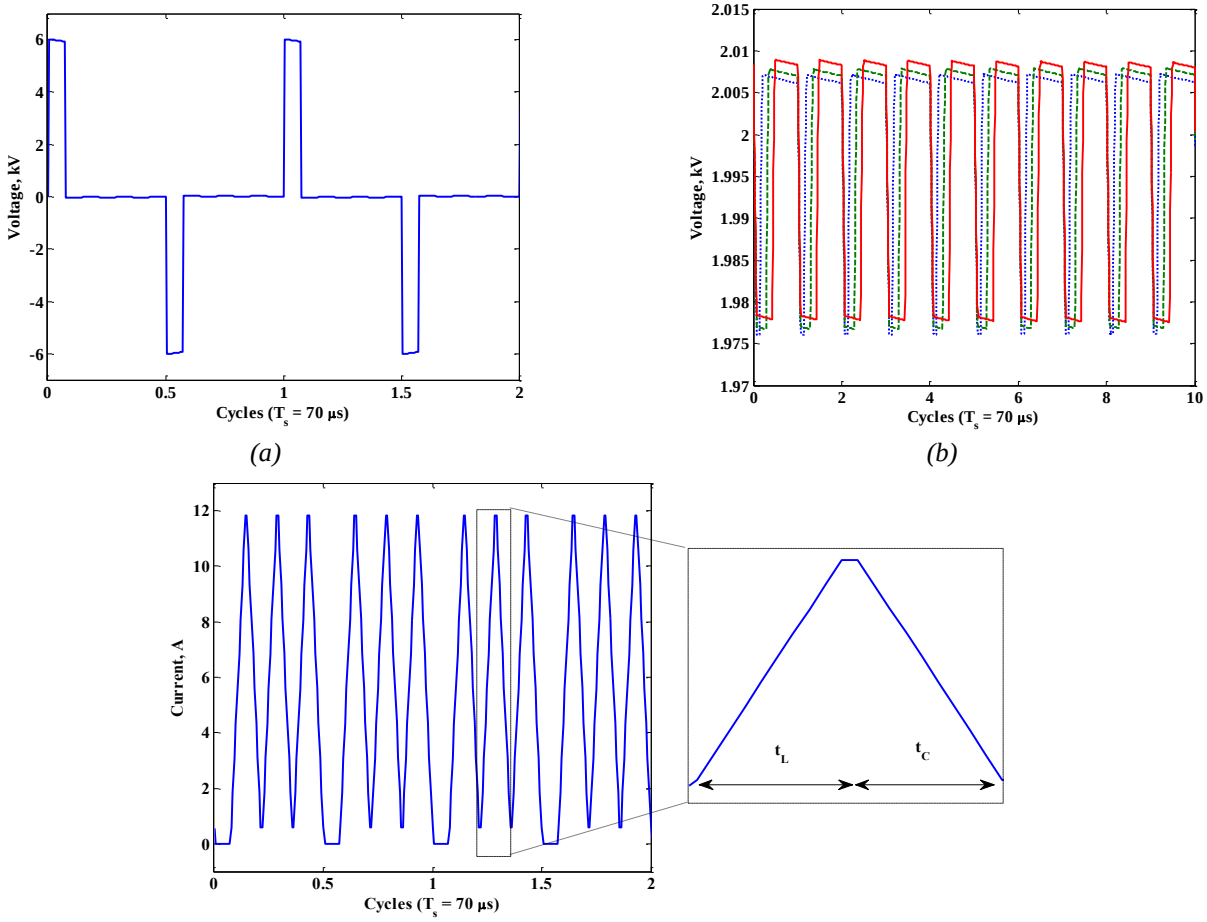


Fig. 6. *Simulation of HV rectangular pulses generated by BMPG for a boost factor $\lambda = 2$*
(a) Voltage pulses, **(b)** Arm1 SM-capacitor voltages, and (c) Input inductor current

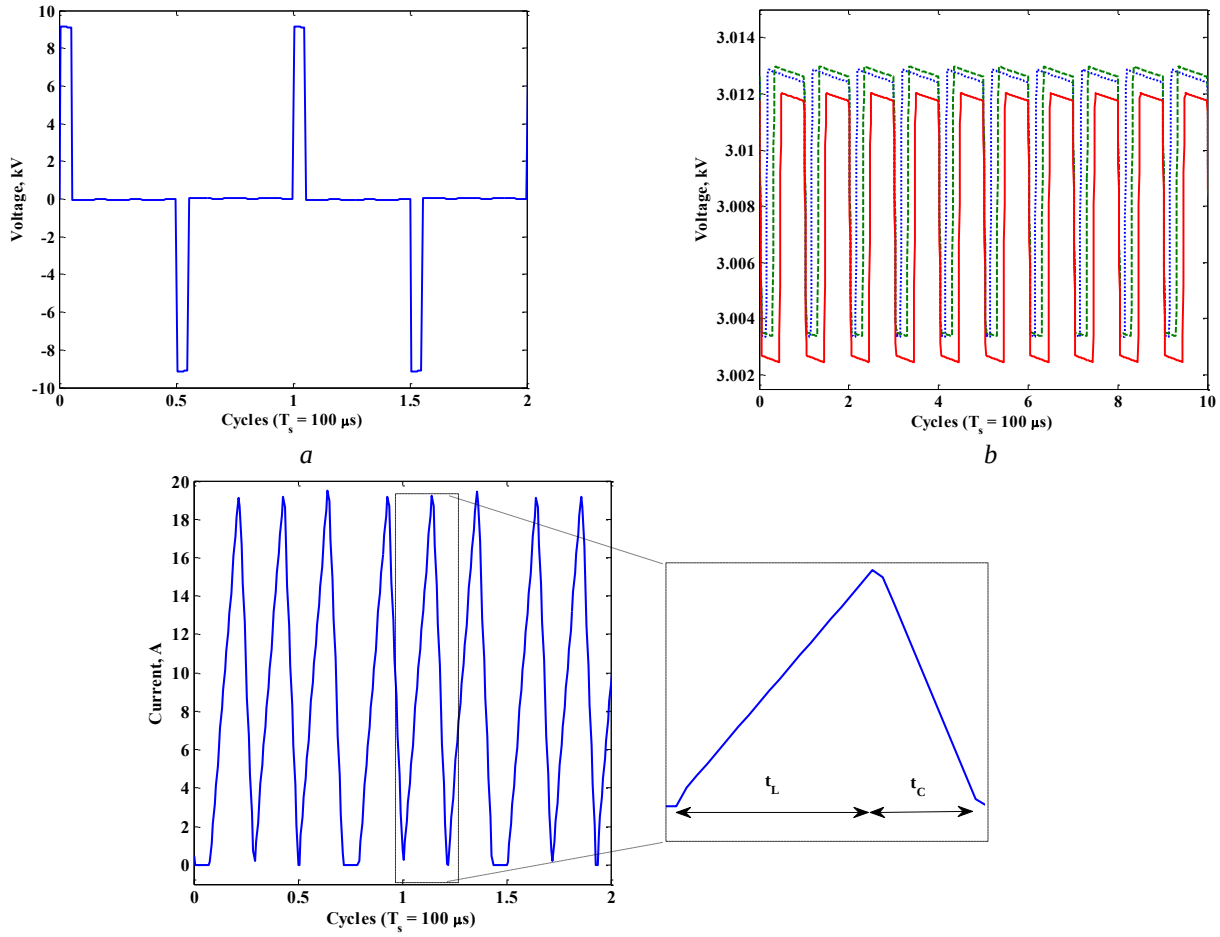
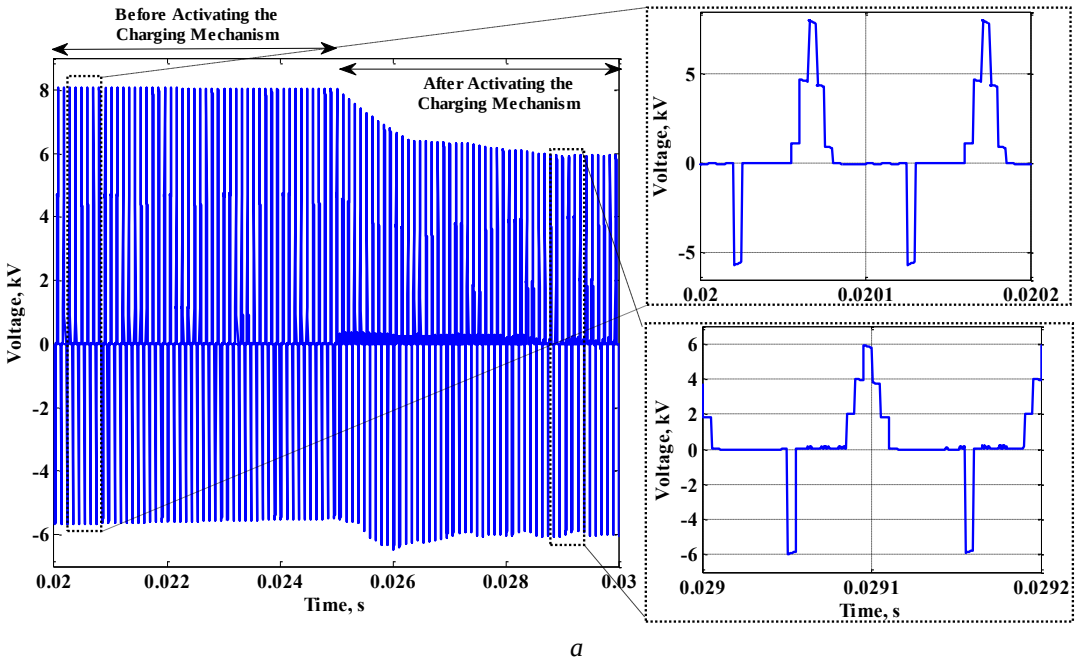


Fig. 7. *Simulation of HV rectangular pulses generated by BMPG for a boost factor* $\lambda = 3$
(a) Voltage pulses, **(b)** Arm1 SM-capacitor voltages and (c) Input inductor current



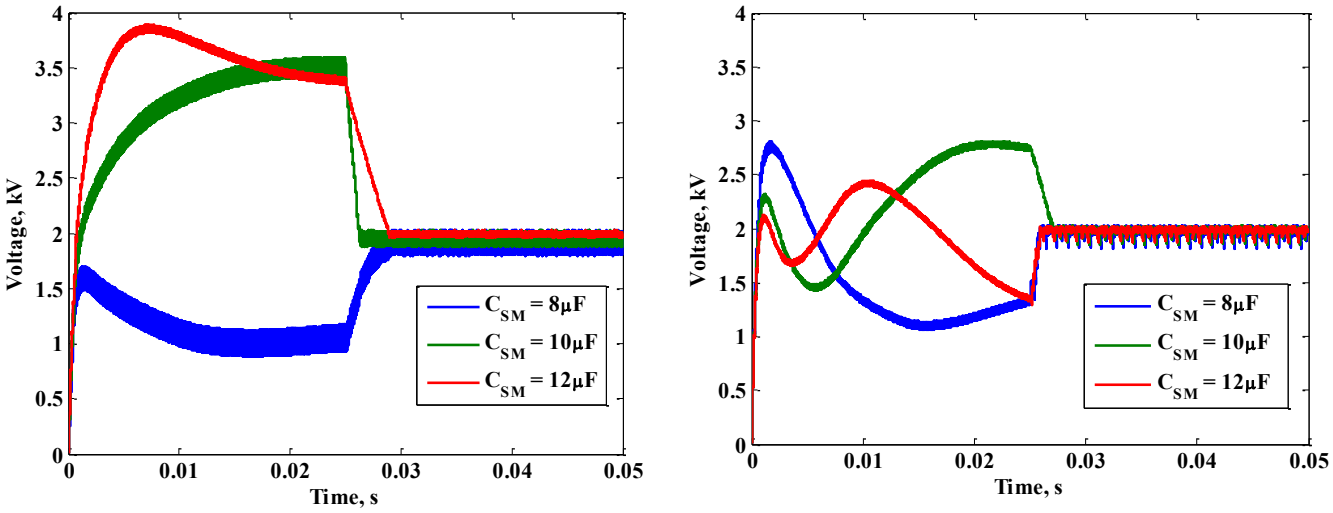


Fig. 8. *Simulation of HV rectangular pulses generated by BMPG for a boost factor* $\lambda = 2$
(a) Voltage pulses, **(b)** Arm1 SM-capacitor voltages, and **(c)** Arm2 SM-capacitor voltages

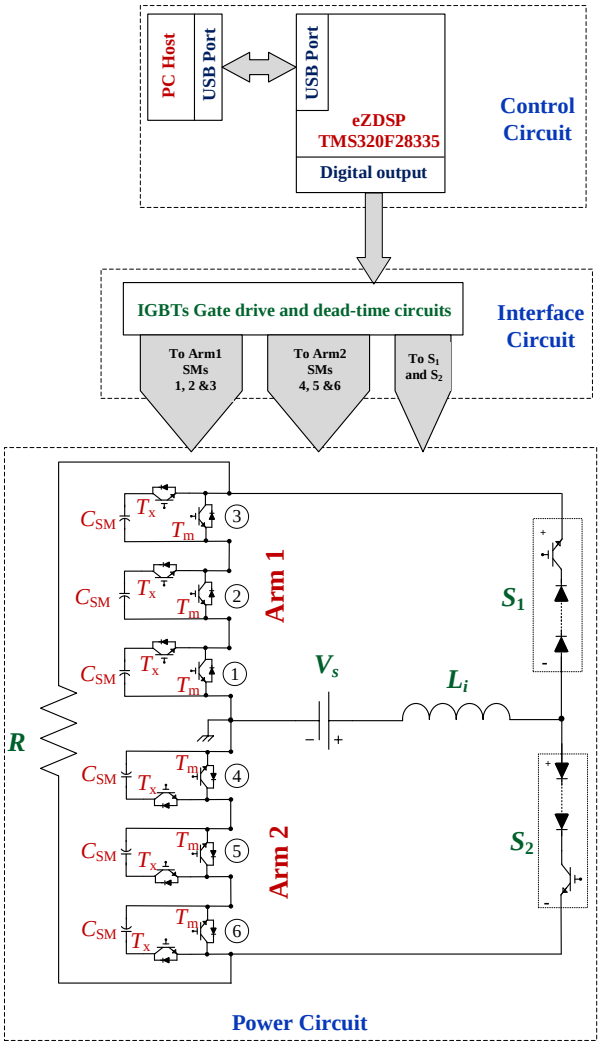


Fig. 9. *Schematic diagram for the experimental set-up with 6 MMC-HB SMs.*

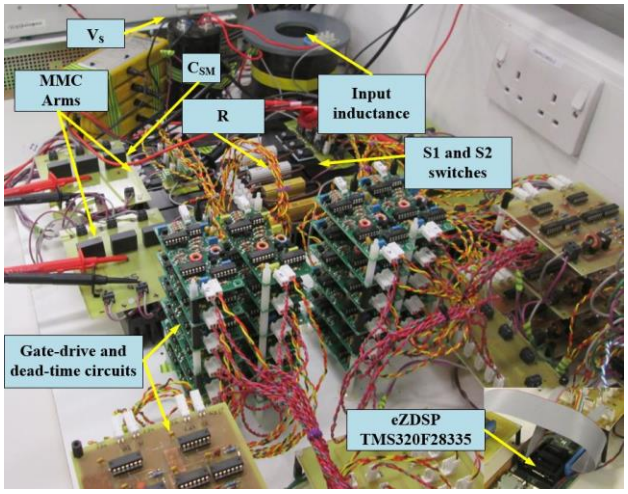


Fig. 10. *BMPG scaled-down proof of concept experimental set-up.*

After activating the proposed charging mechanism, the capacitor voltages balance regardless of their capacitance difference and the experienced voltage drift is alleviated. The simulated capacitance deviation is higher than the practical capacitance values deviation (typically 5% for plastic types), such that the control algorithm is tested at an extreme condition.

4. BMPG Experimental Results

The proof of concept scaled-down experimental schematic diagram as well as the hardware set-up are shown in Fig. 9 and Fig. 10, respectively. The SM IGBT switches in Arm1 and Arm2 are STGW30NC60WD, which have antiparallel diodes, while the reverse blocking switches S1 and S2 are Infineon IGW60T120 IGBTs in series with IXYS DSEI30-10A diodes.

The experimental results are shown in Fig. 11 and Fig. 12 for boost factors $\lambda = 2$ and 3, respectively. The generated voltage pulses are shown in Fig. 11a and Fig. 12a, where for the same input DC voltage, the output voltage is doubled and tripled. Thus, the pulse peak voltage for $\lambda = 2$

is $V_P = 300$V as shown in Fig. 11a, and $V_P = 440$V in Fig. 12a, for $\lambda = 3$. The repetition rate is reduced in the tripled case as more time is required to energize the inductor. $T_s = 260\mu s$ when $\lambda = 2$ and $400\mu s$ when $\lambda = 3$. For both cases the voltages of Arm2 capacitors are shown in Fig. 11b and Fig. 12b for $\lambda = 2$ and $\lambda = 3$, respectively. Individual capacitor voltages are balanced around 150V.

Finally, the inductor input current is depicted in Fig. 11c and Fig. 12c for $\lambda = 2$ and 3, respectively. For $\lambda = 2$, the assigned time for energizing the inductor and charging a capacitor are equal, while the energizing time is double the capacitor charging time when $\lambda = 3$.

5. Conclusion

Aiming at addressing the limitations of LVDC fed rectangular waveform PGs (both the classical and sequential charging MMC topologies), this paper presented a new capacitor sequential charging technique. The charging technique reduces the converter size by charging each SM individually to λV_s such that $\lambda \geq 1$ is a controllable voltage-boost factor.Then the charged capacitors are inserted in series across the load terminals, generating a pulse peak of $\lambda N V_s$. Each SM forms a boost converter with the input supply and a charging inductor. The BMPG generates controllable bipolar rectangular HV pulses for pulsed electric field applications. The BMPG can operate in a multilevel pulse generation mode which can be used to generate different pulse waveform shapes. To avoid capacitor voltage drift, a voltage sensor is added across each arm and the measured voltage is feedback to the software controller which insures capacitor voltage balance. The proposed converter utilizes commercially available semi-conductors. The proposed boost technique was verified by simulations and scaled-down experimentation.

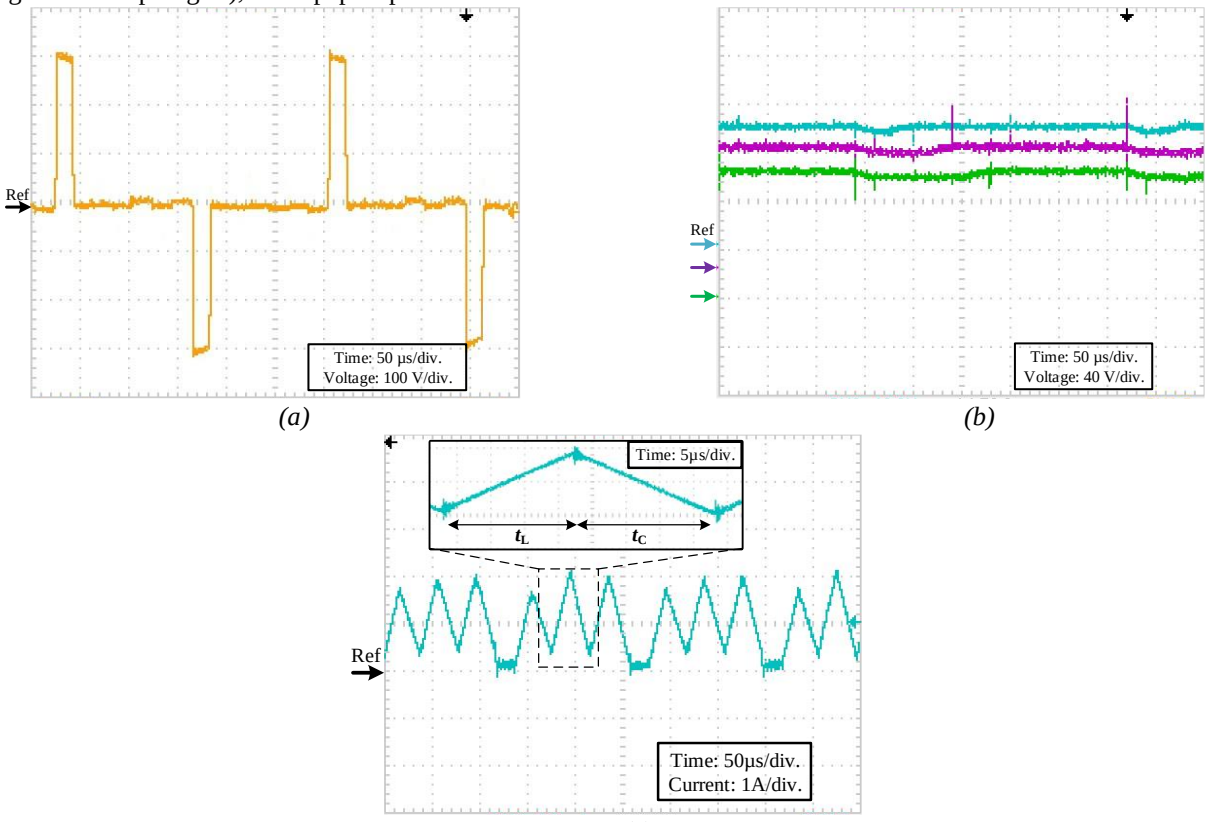
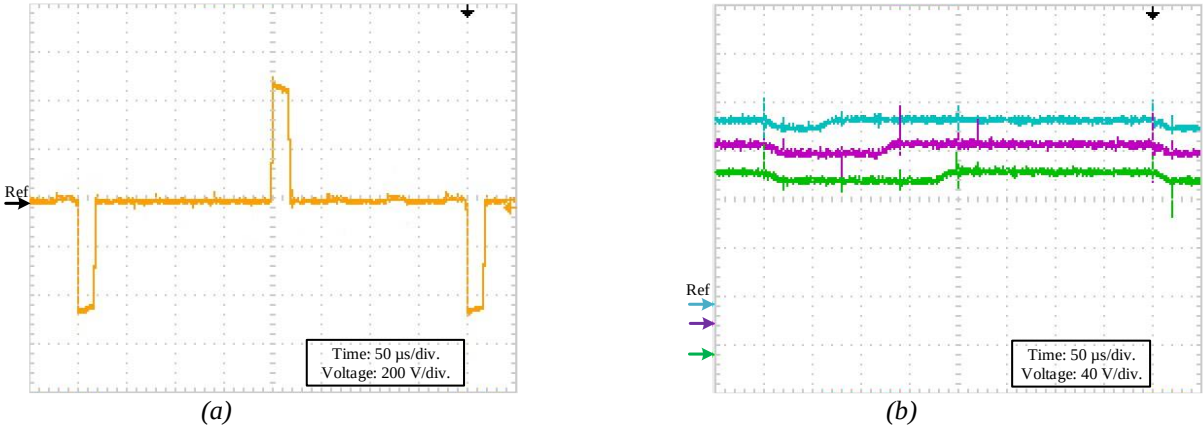
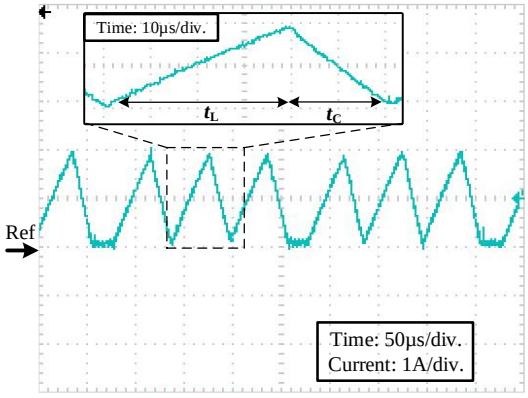


Fig. 11. *BMPG experimental results for a boost factor* $\lambda = 2$
(a) Voltage pulses, **(b)** Arm1 SM-capacitor voltages, and **(c)** Input inductor current.





(c)

Fig. 12. *BMPG experimental results for a boost factor* $\lambda = 3$
(a) Voltage pulses, **(b)** Arm1 SM-capacitor voltages, and **(c)** Input inductor current.

6. Acknowledgments

This work was supported by a National Priorities Research Program (NPRP) grant NPRP (7-203-2-097) from the Qatar National Research Fund (QNRF).

7. References

[1] Schoenbach, K.H., Joshi, R.P., Stark, R.H., Dobbs, F.C., and Beebe, S.J.: 'Bacterial decontamination of liquids with pulsed electric fields', *IEEE Trans. Dielect. Elect. Insulation*, 2000, **7**, (5), pp. 637-645

[2] Bai-Lin, Q., Qinghua, Z., Barbosa-Canovas, *et al*.: 'Inactivation of microorganisms by pulsed electric fields of different voltage waveforms', *IEEE Trans. Dielect. Elect. Insulation*, 1994, **1**, (6), pp. 1047-1057

[3] Bluhm, H.: 'Pulsed power: principles and applications' (Berlin. Springer, 2006. 2006)

[4] Clementson, J., Rahbarnia, K., Grulke, O., *et al*.: 'Design of A, B, and C pulse forming networks using the VINPFN application', *IEEE Trans. Power Electron.*, 2014, **29**, (11), pp 5673-5679

[5] Geun-Hie, R., Pavlov, E.P., Hong-Sik, *et al*.: 'Pulse forming lines for square pulse generators', *IEEE Trans. Plasma Sci.*, 2003, **31**, (2), pp 196-200

[6] Mohsenzade, S., Zarghany, M., Aghaei, M., *et al*.: 'A High-Voltage Pulse Generator With Continuously Variable Pulsewidth Based on a Modified PFN', *IEEE Trans. Plasma Sci.*, 2017, **45**, (5), pp 849-858.

[7] Tewari, S.V., Umbarkar, S.B., Agarwal, R., *et al*.: 'Development and analysis of PFN based compact Marx generator using finite integration technique for an antenna load', *IEEE Trans. Plasma Sci*., 2013, **41**, (10), pp 2684-2690

[8] Canacsinh, H., Redondo, L.M., and Silva, J.F.: 'Marx-Type Solid-State Bipolar Modulator Topologies: Performance Comparison', *IEEE Trans. Plasma Sci.*, 2012, **40**, (10), pp. 2603-2610

[9] Redondo, L.M.: 'New four-switches bipolar solid-state Marx generator', in *2013 19th IEEE Pulsed Power Conference (PPC)*, 2013, pp. 1-5

[10] Yao, C., Zhang, X., Guo, F., *et al*.: 'FPGA-Controlled All-Solid-State Nanosecond Pulse Generator for Biological Applications', *IEEE Trans. Plasma Sci.*, 2012, **40**, (10), pp. 2366-2372

[11] Shi, H., Lu, Y., Gu, T.,*et al*.: 'High-voltage pulse waveform modulator based on solid-state Marx generator', *IEEE Trans. Dielectr. Electr. Insul.*, 2015, **22**, (4), pp. 1983-1990

[12] Veilleux, E., Ooi, B.T., and Lehn, P.W.: 'Marx dc-dc converter for high-power application', *Power Electronics, IET*, 2013, **6**, (9), pp 1733-1741

[13] Sakamoto, T., Nami, A., Akiyama, M., *et al*.: 'A repetitive solid state marx-type pulsed power generator using multistage switch-capacitor cells', *IEEE Trans. Plasma Sci*., 2012, **40**, (10), pp 2316-2321

[14] Redondo, L.M., Silva, J.F., Tavares, P.,*et al*: 'High-voltage high-frequency Marx-bank type pulse generator using integrated power semiconductor half-bridges', in *2005 European Conference on Power Electronics and Applications*, 2005

[15] Canacsinh, H., Silva, J.F., and Redondo, L.M.: 'Dual Resonant Voltage Droop Compensation for Bipolar Solid-State Marx Generator Topologies', *IEEE Trans. Plasma Sci*., 2018, pp. 1-7

[16] Redondo, L.M., and Silva, J.F.: 'Flyback versus forward switching power supply topologies for unipolar pulsed-power applications', *IEEE Trans. Plasma Sci.*, 2009, **37**, (1), pp. 171-178

[17] Davari, P., Zare, F., Ghosh, A., *et al*: 'High-voltage modular power supply using parallel and series configurations of flyback converter for pulsed power applications', *IEEE Trans. Plasma Sci.*, 2012, **40**, (10), pp. 2578-2587

[18] Zabihi, S., Zare, F., Ledwich, G., *et al*:: 'A novel high-voltage pulsed-power supply based on low-voltage switch-capacitor units', *IEEE Trans. Plasma Sci.*, 2010, **38**, (10), pp. 2877-2887

[19] Delshad, M.R., Rezanejad, M., and Sheikholeslami, A.: 'A New Modular Bipolar High-Voltage Pulse Generator', *IEEE Trans. Ind. Electron.*, 2017, **64**, (2), pp. 1195-1203

[20] Rezanejad, M., Sheikholeslami, A., and Adabi, J.: 'High-Voltage Modular Switched Capacitor Pulsed Power Generator', *IEEE Trans. Plasma Sci.*, 2014, **42**, (5), pp. 1373-1379.
[21] Rocha, L.L., Silva, J.F., and Redondo, L.M.: 'Seven-level unipolar/bipolar pulsed power generator', *IEEE Trans. Plasma Sci.*, 2016, **44**, (10), pp 2060-2064
[22] Rocha, L.L., Silva, J.F., and Redondo, L.M.: 'Multilevel high-voltage pulse generation based on a new modular solid-state switch', *IEEE Trans. Plasma Sci*., 2014, **42**, (10), pp 2956-2961
[23] Elserougi, A.A., Massoud, A.M., and Ahmed, S.: 'Modular multilevel converter-based bipolar high-voltage pulse generator with sensorless capacitor voltage balancing technique', *IEEE Trans. Plasma Sci*., 2016, **44**, (7), pp 1187-1194
[24] Elgenedy, M.A., Darwish, A., Ahmed, S., *et al.*: 'A modular multilevel-based high-voltage pulse generator for water disinfection applications', *IEEE Trans. Plasma Sci*., 2016, **44**, (11), pp 2893-2900
[25] Elgenedy, M.A., Darwish, A., Ahmed, S., *et al.*: 'A transition arm modular multilevel universal pulse-waveform generator for electroporation applications', *IEEE Trans. Power Electron.*, 2017, **32**, (12), pp 8979-8991
[26] Elserougi, A.A., Faiter, M., Massoud, A.M., *et al*.: 'A transformer-less bipolar/unipolar high-voltage pulse generator with low-voltage components for water treatment applications', *IEEE Trans. Ind. Applicat.*, 2017, to be published
[27] Elserougi, A.A., Massoud, A.M., and Ahmed, S.: 'A modular high-voltage pulse-generator with sequential charging for water treatment applications', *IEEE Trans. Ind. Electron*., 2016, **63**, (12), pp 7898-7907
[28] Elserougi, A.A., Abdelsalam, I., Massoud, A.M., *et al*.: 'A full-bridge submodule-based modular unipolar/bipolar high-voltage pulse generator with sequential charging of capacitors', *IEEE Trans. Plasma Sci.*, 2017, **45**, (1), pp 91-99
[29] Elserougi, A., Massoud, A., and Ahmed, S.: 'Conceptual study of a bipolar modular high voltage pulse generator with sequential charging', *IEEE Trans. Dielectr. Electr. Insul.*, 2016, **23**, (6), pp 3450-3457
[30] Elgenedy, M.A., Massoud, A.M., Ahmed, S., *et al*.: 'A high-gain, high-voltage pulse generator using sequentially-charged modular multilevel converter sub-modules, for water disinfection applications', *IEEE Journal. Emerg. Select. Topics in Power Electronics*, 2018, **6**, (3), pp. 1394-1406